RDA5800C

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.4.1–Oct.2007

1   General Description

The RDA5800C is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5800C has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

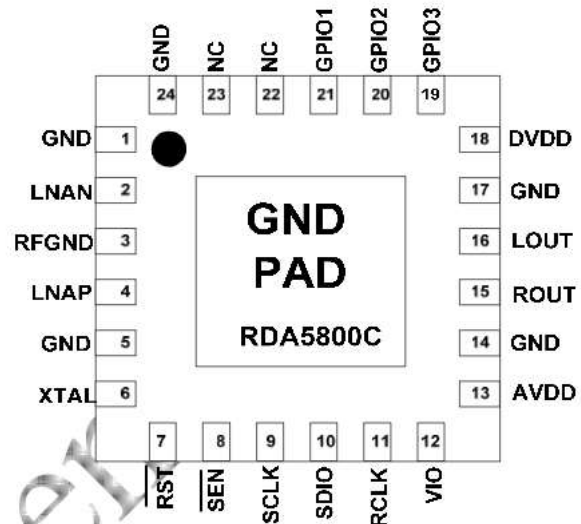The RDA5800C can be tuned to the worldwide frequency band.

Figure 1-1. RDA5800C Top View

1.1   Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 16mA at 3.3V power supply
- Support worldwide frequency band
  - 76 -108 MHz
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute

- High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI)
- Bass boost
- Analog and digital volume control
- I^2S digital output interface
- Line-level analog output voltage
- 32.768 KHz reference clock
- 2-wire and 3-wire serial control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 2.7 to 5.5 V operation voltage
- 4X4mm 24 pin QFN package

1.2   Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook PCs

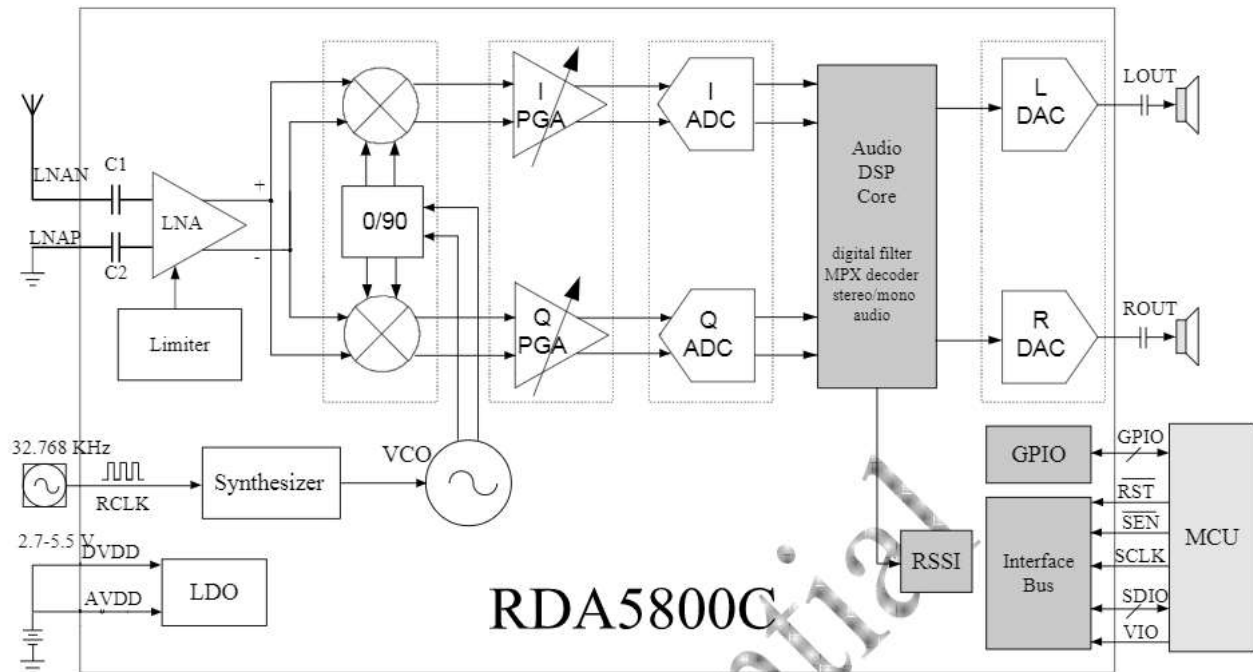## 2   Table of Contents

3   Functional Description

Figure 3-1. RDA5800C FM Tuner Block Diagram

3.1   FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (76 to 108MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNAN) and supports any input port by set according registers bits (LNA_PORT_SEL[1:0]). The LNA default input resistance is 150 Ohm under single or dual input mode. It default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

3.2   Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 76MHz to 108MHz.

3.3   Power Supply

The RDA5800C integrated one LDO which supplies power to the chip. The external supply voltage range is 2.7-5.5 V.

3.4   Powerdown and Reset

The RDA5800C selects three-wire or I^2C control interface in reset process. Setting $\overline{RST}$ pin low after power up will reset the chip to initial state. Setting $\overline{RST}$ pin high will bring the chip out of reset. Setting $\overline{SEN}$ low on the rising edge of $\overline{RST}$ will select three-wire control interface, and setting $\overline{SEN}$ high on the rising edge of $\overline{RST}$ will select I^2C control interface.
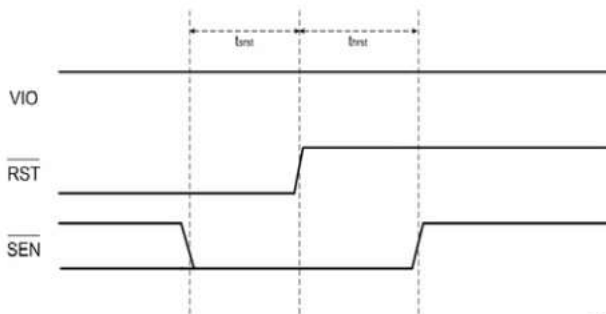

Figure 3-1. Three-wire Interface Reset Timing Diagram

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{SEN}$ Input to $\overline{RST}$ ↑ Setup	tsrst		30			ns
$\overline{SEN}$ Input to $\overline{RST}$ ↑ Hold	thrst		30			ns

Table 3-1 SPI Reset Timing Characteristics
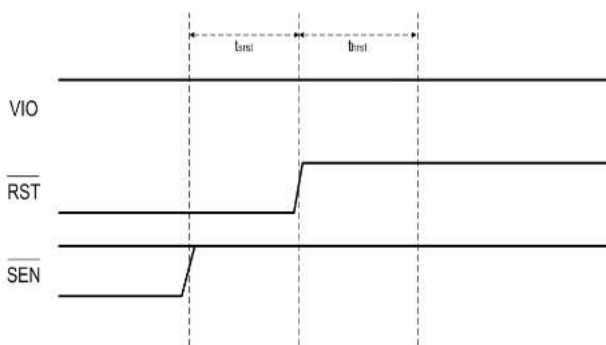
Figure 3-2. I2C Interface Reset Timing Diagram

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{SEN}$ Input to $\overline{RST}$ ↑ Setup	tsrst		30			ns
$\overline{SEN}$ Input to $\overline{RST}$ ↑ Hold	thrst		30			ns

Table 3-2 I2C Reset Timing Characteristics

When need, the RDA5800C could enter into a powerdown mode to reduce power consumption, with software setting the ENABLE bit low. In powerdown mode, analog and digital circuitry are both disabled, while maintaining register configuration and keeping control interface active. The RDA5800C could enter back into normal mode by setting the ENABLE bit high, and resume normal working.

Details refer to *RDA5800 Programming Guide*.

3.5   Control Interface

The RDA5800C supports three-wire and I^2C control interface. User could select either of them to program the chip.

The three-wire interface is a standard SPI interface. It includes three pins: $\overline{SEN}$, SCLK and SDIO. Each register write is 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit). RDA5800C samples command byte and data at posedge of SCLK. Each register read is also 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit) from RDA5800C. The turn around cycle between command byte from MCU and data from RDA5800C is a half cycle. RDA5800C samples command byte at posedge of SCLK, and output data also at posedge of SCLK.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5800C. There is no visible register address in I^2C interface transfers. The I^2C

interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5800 always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5800 sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5800 will return the bus to MCU, and MCU will give out STOP condition.

Details refer to *RDA5800 Programming Guide*.

3.6   I²S Audio Data Interface

The RDA5800C supports I²S (Inter_IC Sound Bus)

audio interface. The interface is fully compliant with I²S bus specification. When setting I2SEN bit high, RDA5800C will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I²S master and transmitter, the sample rate is 42Kbps.

3.7   GPIO Outputs

The RDA5800C has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST. Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE bit.

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
AVDD	Analog Supply Voltage	2.7	3.3	5.5	V
DVDD	Digital Supply Voltage	2.7	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current [1]	-10		+10	mA
V_{IN}	Input Voltage [1]	-0.3		VIO+0.3	V
V_{Ina}	LNA FM Input Level			-20	dBm

Notes:

1. For Pin: SCLK, SDIO, $\overline{SEN}$, $\overline{RST}$.

Table 4-3 Power Consumption Specification

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_A	Analog Supply Current	ENABLE=1	13	mA
I_D	Digital Supply Current	ENABLE=1	3	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	1	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	2	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	2	μA

5   Receiver Characteristics

Table 5-1   Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency	BAND=0	87.5		108	MHz
		BAND=1	76		91	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1.5	2	μV EMF
R_{in}	LNA Input Resistance [7]		130	150	170	Ω
C_{in}	LNA Input Capacitance [7]		2	4	6	pF
$IP3_{in}$	Input IP3[4]	AGCD=1	80		-	dBμV
$α_{am}$	AM Suppression[1,2]	m=0.3	40	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz	45	-	-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume_dsp[3:0]=1111 Volume_dac[3:0] =1111	60	75	90	mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		54	60	-	dB
$α_{SCS}$	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.3	0.5	%
$α_{AOI}$	Audio Output L/R Imbalance				1	dB
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
Pins LNAN, LNAP, LOUT, ROUT and NC(22,23)						
V_{com_rfin}	Pins LNAN and LNAP Input Common Mode Voltage			Float		V
V_{com}	Audio Output Common Mode Voltage[8]		0.9	1	1.1	V
V_{com_nc}	Pins NC (22, 23) Common Mode Voltage		0.45	0.5	0.55	V
! The NC(22, 23) pins SHOULD BE left floating.						

Notes:

1. F_{in}=76 to 108MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;

2. Δf=22.5KHz;

3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;

4. |f_2-f_1|>1MHz, f_0=2xf_1-f_2, AGC disable, F_{in}=76 to 108MHz;

5. P_{RF}=60dB$_U$V;

6. Δf=75KHz.

7. Measured at V_{EMF} = 1 m V, f_{RF} = 76 to 108MHz

8. At LOUT and ROUT pins

6   Serial Interface

6.1   Three-wire Interface Timing

Table 6-1   Three-wire Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

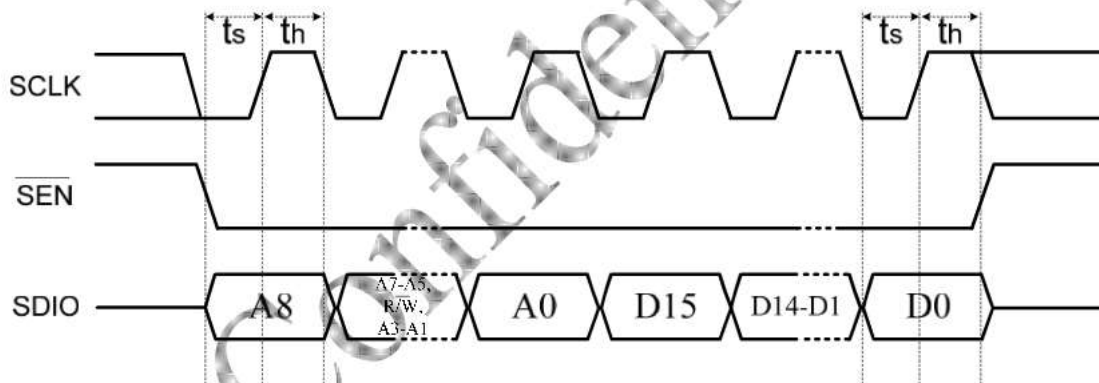| PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Cycle Time	t_{CLK}		35			ns
SCLK Rise Time	t_R				50	ns
SCLK Fall Time	t_F				50	ns
SCLK High Time	t_{HI}		10			ns
SCLK Low Time	t_{LO}		10			ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_s		10	-	-	ns
SDIO Input, to SCLK↑ Hold	t_h		10	-	-	ns
SCLK↑ to SDIO Output Valid	t_{cdv}	Read	2	-	10	ns
$\overline{SEN}$↑ to SDIO Output High Z	t_{sdz}	Read	2	-	10	ns
Digital Input Pin Capacitance					5	pF

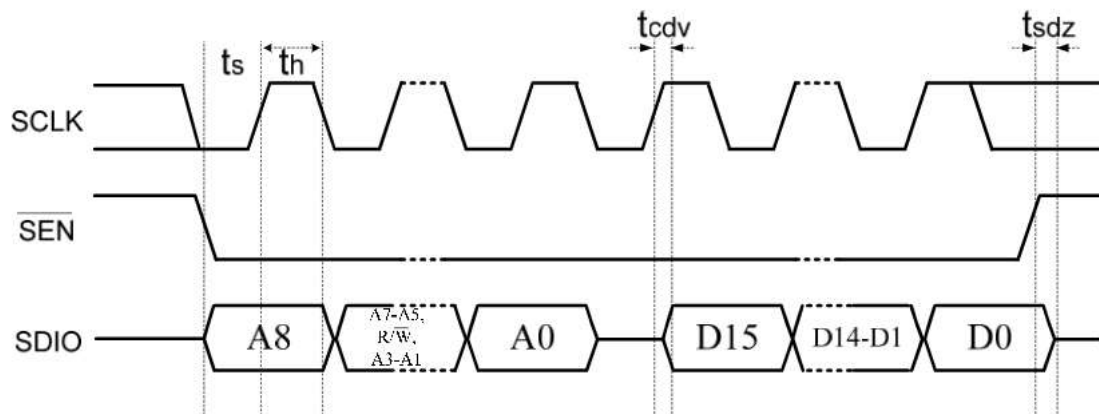Figure 6-1. Three-wire Interface Write Timing Diagram

Figure 6-2. Three-wire Interface Read Timing Diagram

6.2   I^{2}C Interface Timing

Table 6-2   I^{2}C Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T$_A$ = -25 to 85 °C, unless otherwise specified)

| PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF
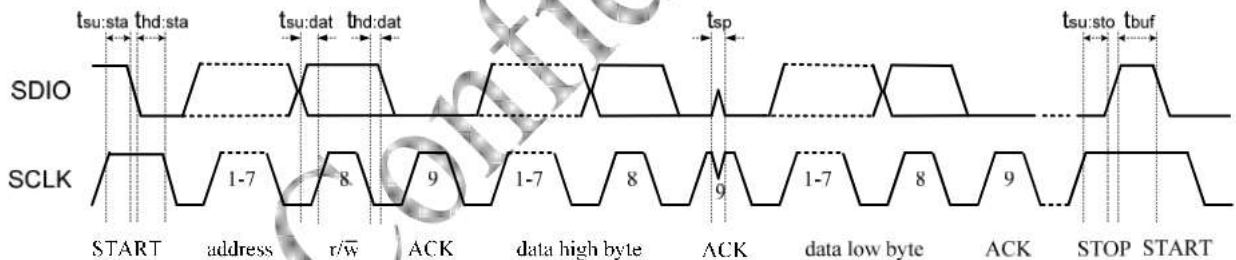
Figure 6-3. I^{2}C Interface Write Timing Diagram
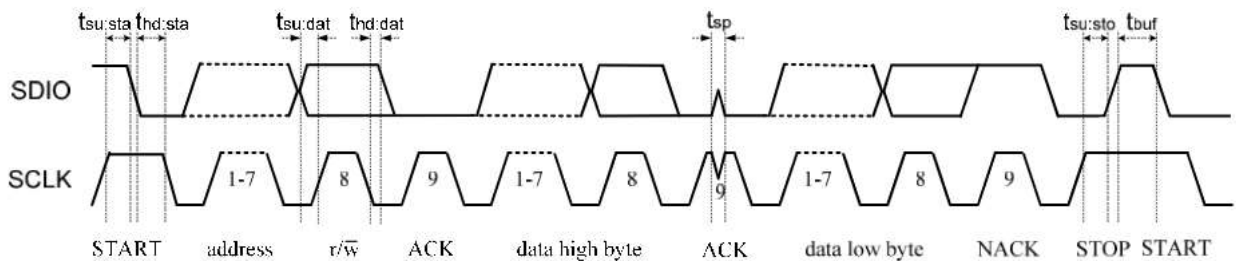
Figure 6-4. I^{2}C Interface Read Timing Diagram

7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. *0 = High impedance; 1 = Normal operation*	0
	14	DMUTE	Mute Disable. *0 = Mute; 1 = Normal operation*	0
	13	MONO	Mono Select. *0 = Stereo; 1 = Force mono*	0
	12	BASS	Bass Boost. *0 = Disabled; 1 = Bass boost enabled*	0
	9	SEEKUP	Seek Up. *0 = Seek down; 1 = Seek up*	0
	8	SEEK	Seek. *0 = Disable; 1 = Enable* *Seek begins in the direction specified by SEEKUP and ends when a channel is found with RSSI level above SEEKTH[5:0], or the entire band has been searched.* *The SEEK bit is set low and the STC bit is set high when the seek operation completes.*	0
	0	ENABLE	Power Up Enable. *0 = Disabled; 1 = Enabled*	0
03H	15:8	CHAN[7:0]	Channel Select. BAND = 0 *Frequency =* *Channel Spacing (kHz) x CHAN+ 87.5 MHz* BAND = 1 *Frequency =* *Channel Spacing (kHz) x CHAN + 76.0 MHz* *CHAN is updated after a seek operation.*	0x00
	2	SPACE_50K	Channel Spacing. *0 = see SPACE bit; 1 = 50 kHz*	0
	1	BAND	Band Select. *0 = 87.5-108 MHz (US/Europe)* *1 = 76-91 MHz (Japan)*	0
	0	SPACE	Channel Spacing. *0 = 100 kHz; 1 = 200 kHz*	0
04H	14	STCIEN	Seek/Tune Complete Interrupt Enable. *0 = Disable Interrupt; 1 = Enable Interrupt* *Setting STCIEN = 1 will generate a 5 ms low pulse on GPIO2 when the interrupt occurs.*	0
	11	DE	De-emphasis. *0 = 75 µs; 1 = 50 µs*	0
	6	I2SEN	I²S Bus Enable. *0 = disabled; 1 = enabled.*	0
	5:4	GPIO3[1:0]	General Purpose I/O 3. *00 = High impedance* *01 = Mono/Stereo indicator (ST)*	00

| REG	BITS	NAME	FUNCTION	DEFAULT
			10 = Low 11 = High	
	3:2	GPIO2[1:0]	General Purpose I/O 2. 00 = High impedance 01 = Interrupt (INT) 10 = Low 11 = High	00
	1:0	GPIO1[1:0]	General Purpose I/O 1. 00 = High impedance 01 = Reserved 10 = Low 11 = High	00
05H	15	INTMODE	INT Mode Select. 0 = Generate 5ms interrupt; 1 = Interrupt last until write action occurs.	0
	13:8	SEEKTH[5:0]	Seek Threshold in Logarithmic. 000000 = min RSSI; 111111 = max RSSI	000100
	7:4	VOLUME_DSP[3:0]	DSP Volume Control. 0000=min -15db; 1111=max 0db	1111
	3:0	VOLUME_DAC[3:0]	DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic	0000
0AH	14	STC	Seek/Tune Complete. 0 = Not complete; 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	0
	13	SF	Seek Fail. 0 = Seek successful; 1 = Seek failure The seek fail flag is set when the seek operation fails to find a channel with an RSSI level greater than SEEKTH[5:0].	0
	8	ST	Stereo Indicator. 0 = Mono; 1 = Stereo Stereo indication is available on GPIO3 by setting GPIO1[1:0] =01.	1
	7:0	READCHAN[7:0]	Read Channel. BAND = 0 Frequency = Channel Spacing (kHz) x READCHAN + 87.5 MHz BAND = 1 Frequency = Channel Spacing (kHz) x READCHAN + 76.0 MHz READCHAN is updated after a tune or seek operation.	0x00
0BH	13:8	RSSI	RSSI in Logarithmic. 000000 = min; 111111 = max	0x00
10H	14:13	LNA_PORT_SEL[1:0]	LNA input port selection bit. 01 = LNAN input 10 = LNAP input 11 = dual port input	10

8   Pins Description
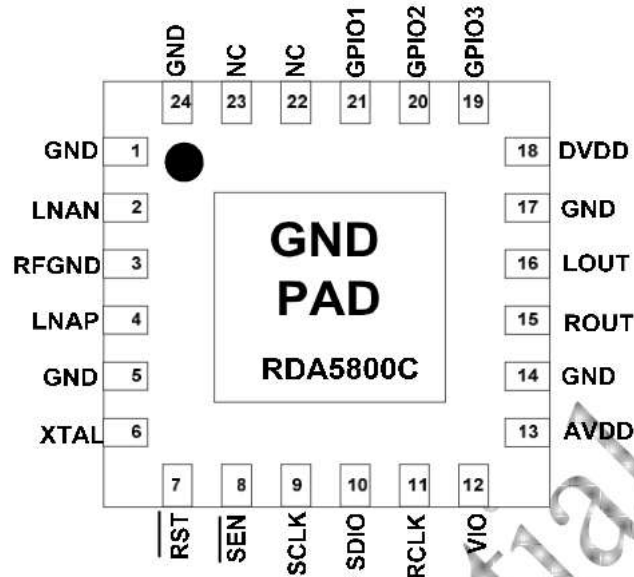
Figure 0-1. RDA5800C Top View

Table 0-1   RDA5800C Pins Description

SYMBOL	PIN	DESCRIPTION
GND	1,5,14,17,24	Ground. Connect to ground plane on PCB
LNAN,LNAP	2,4	LNA input port. For single-ended input, LNAN should be connected to RFGND
RFGND	3	LNA ground. Connect to ground plane on PCB
XTAL	6	Crystal oscillator input.
$\overline{RST}$	7	Latch reset (active low) input for serial control bus
$\overline{SEN}$	8	Latch enable (active low) input for serial control bus
SCLK	9	Clock input for serial control bus
SDIO	10	Data input/output for serial control bus
RCLK	11	32.768KHz external reference clock input
VIO	12	Power supply for I/O
AVDD	13	Power supply for analog section
ROUT,LOUT	15,16	Right/Left audio output
DVDD	18	Power supply for digital section
GPIO1,GPIO2,GPIO3	19,20,21	General purpose input/output
NC	22,23	No Connect

9   Application Diagram

9.1   Audio Loading Resistance Larger than 32Ω & TCXO Application:
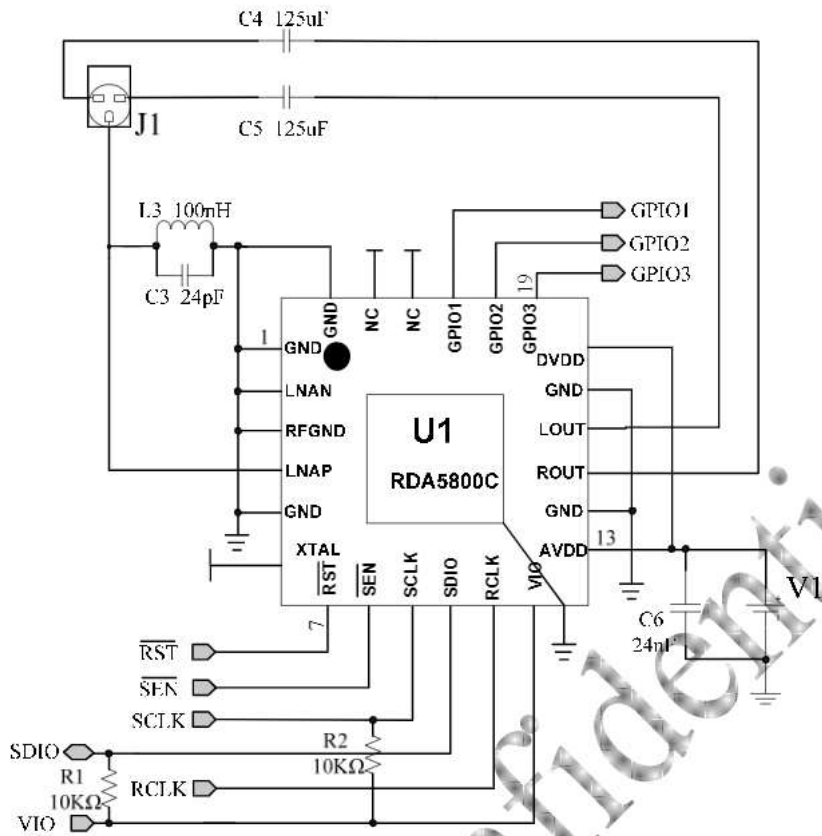
Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5800C Chip;
3. R1,R2 I²C 3-wire Bus Pull-up Resistor;
4. V1: Analog and Digital Power Supply (2.7~5.5V);
5. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
6. Pins NC(22, 23),XTAL Should be Leaved Floating;
7. Place C6 Close to AVDD pin.

Figure 9-1. RDA5800C FM Tuner Application Diagram (TCXO Application)

9.1.1   Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5800C	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
R1,R2	10KΩ	I²C Bus Pull-up Resistor	
L3/C3	100nH/24pF	LC Chock for LNA Input	
C4,C5	125µF	Audio AC Couple Capacitors	
C6	24nF	Power Supply Bypass Capacitor	

9.2   Audio Loading Resistance Lower than 32Ω & TCXO Application:

Notes:

1. J1: Resistance Lower than 32Ω Audio Speaker or Headphone
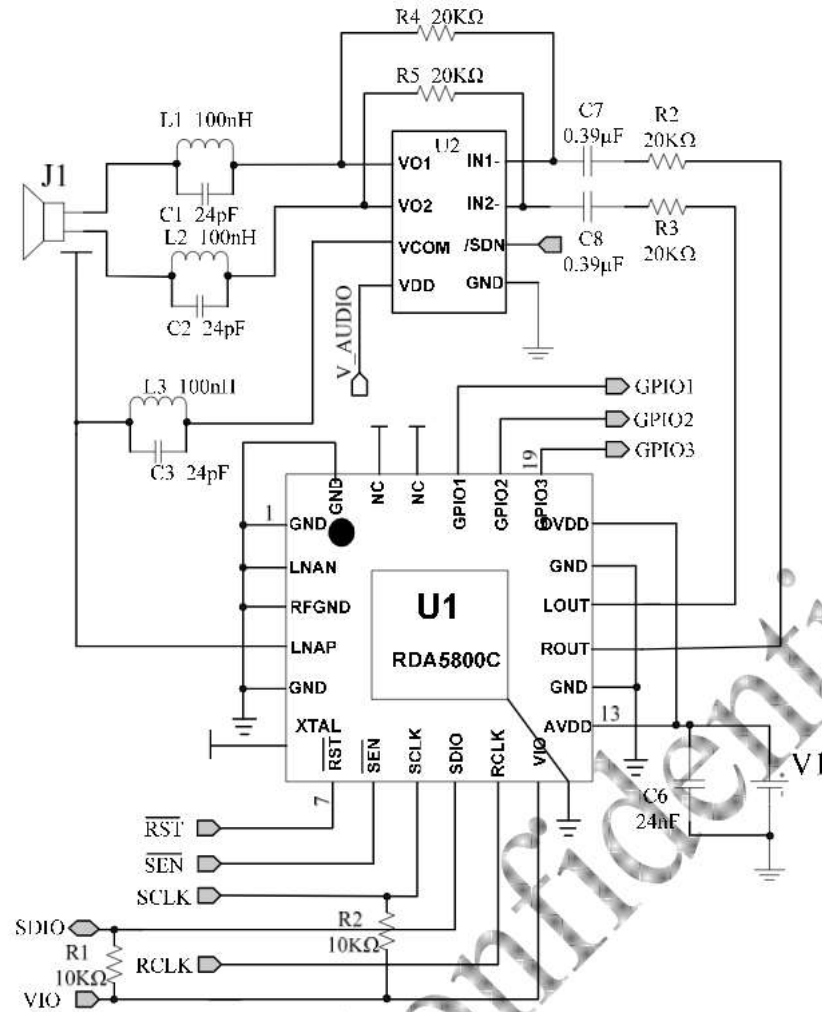2. U1: RDA5800C Chip
3. R1,R2 I^{2}C 3-wire Bus Pull-up Resistor
4. V1: Analog and Digital Power Supply (2.7~5.5V)
5. FM Choke (L3 and C3) for Audio Common and LNA Input Common
6. Pins NC(22, 23),XTAL Should be Leaved Floating
7. Place C6 Close to AVDD pin
8. Changing the Resistor R4 and R5 Value can Change the Output Volume.

Figure 9-2. RDA5800C FM Tuner Application Diagram (Audio Amplifier Application)

9.2.1   Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5800C	Broadcast FM Radio Tuner	RDA
U2		Audio Amplifier	
J1		Audio Speaker	
R1,R2	10KΩ	I^{2}C Bus Pull-up Resistor	
L1/C1; L2/C2	100nH/24pF	LC Chock for Audio Output	
L3/C3	100nH/24pF	LC Chock for LNA Input	
C6	24nF	Power Supply Bypass Capacitor	
R4,R5	20KΩ	Audio Amplifier Feedback Resistors	
R2/C7; R3/C8	20KΩ/0.39µF	Audio High-passed Filter and Amplifier Input Resistors	

9.3 Audio Loading Resistance Larger than 32Ω & DCXO Application:

Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5800C Chip;
3. U2: 32.768KHz Crystal oscillator
4. R1,R2: I^{2}C 3-wire Bus Pull-up Resistor;
4. V1: Analog and Digital Power Supply (2.7~5.5V);
5. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
6. Pins NC(22, 23) Should be Leaved Floating;
7. Place C6 Close to AVDD pin.
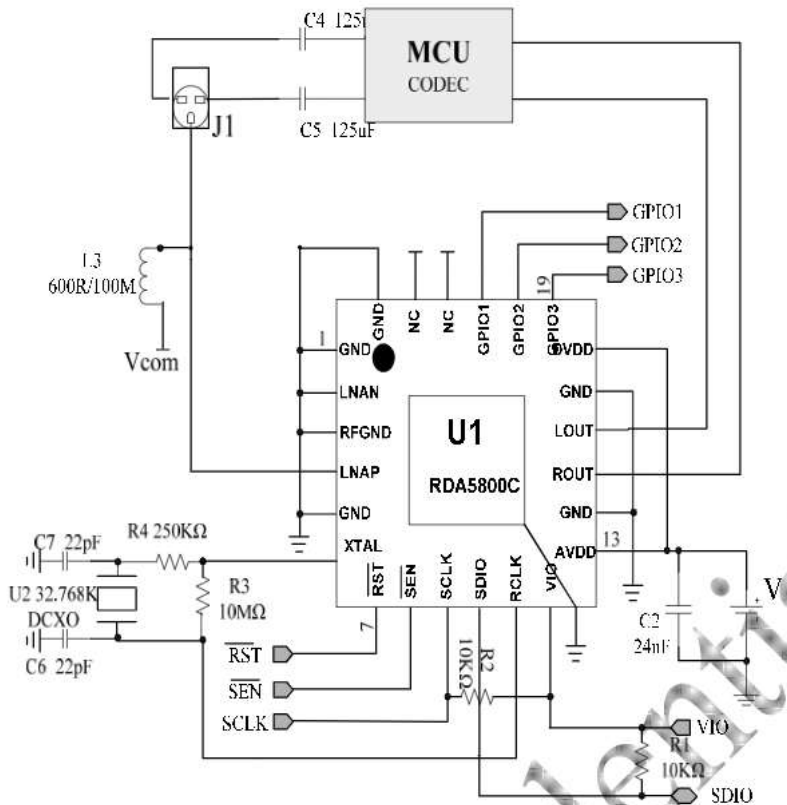8. Load of Crystal oscillator (C6,C7,R3,R2)
9. Place U2 Close to U1

Figure 9-3. RDA5800C FM Tuner Application Diagram (DCXO Application)

9.3.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5800C	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	
J1		Common 32Ω Resistance Headphone	
R1,R2	10KΩ	I^{2}C Bus Pull-up Resistor	
L3/C3	100nH/24pF	LC Chock for LNA Input	
C4,C5	125μF	Audio AC Couple Capacitors	
C2	24nF	Power Supply Bypass Capacitor	
C6,C7	22pF	Load Capacitor of DCXO	
R3,R4	5MΩ/250KΩ	Load Resistor f DCXO	

9.4   MCU CODEC Application:

Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5800C Chip;
3. U2: 32.768KHz Crystal oscillator
4. R1,R2: I²C 3-wire Bus Pull-up Resistor;
4. V1: Analog and Digital Power Supply (2.7~5.5V);
5. FM Choke L3 for LNA Input Common;
6. Pins NC(22, 23) Should be Leaved Floating;
7. Place C6 Close to AVDD pin.
8. Load of Crystal oscillator (C6,C7,R3,R2)
9. Place U2 Close to U1

Figure 9-4. RDA5800C FM Tuner Application Diagram (DCXO+MCU CODEC Application)

9.4.1   Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5800C	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	
J1		Common 32Ω Resistance Headphone	
R1,R2	10KΩ	I²C Bus Pull-up Resistor	
L3	600R/100M	Common for LNA Input	
C4,C5	125µF	Audio AC Couple Capacitors	
C2	24nF	Power Supply Bypass Capacitor	
C6,C7	22pF	Load Capacitor of DCXO	
R3,R4	5MΩ/250KΩ	Load Resistor f DCXO	

10 Package Physical Dimension

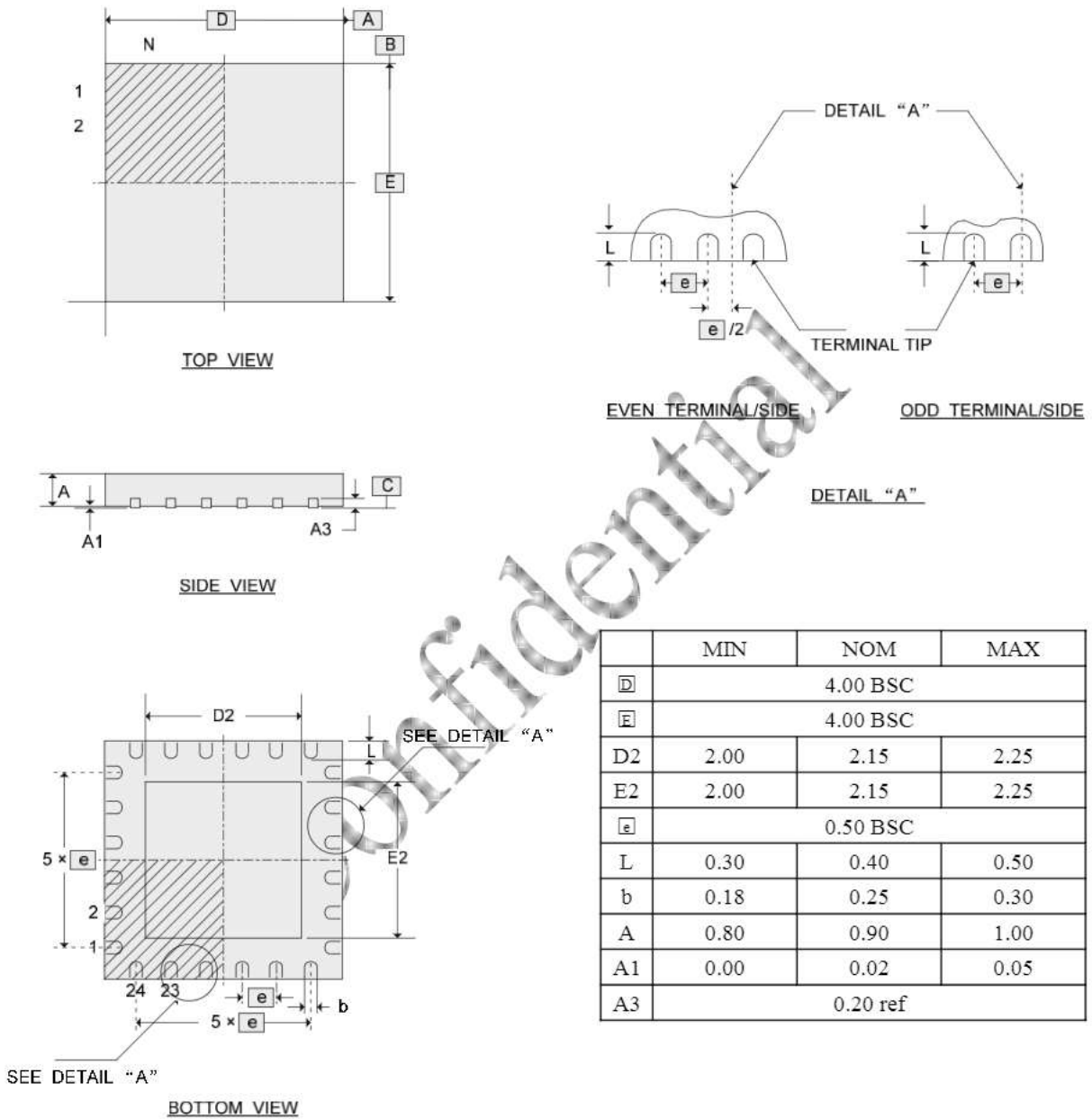*Figure 10-1* illustrates the package details for the RDA5800. The package is lead-free and RoHS-compliant.

	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.00	2.15	2.25
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

Figure 10-2. 24-Pin 4x4 Quad Flat No-Lead (QFN)

11 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2006-11-28	Chun Zhao, Lin Li, Hua Li	Original Draft.
V2.0	2007-03-08	Chun Zhao, XiaoQi You	Up data test result; add DCXO application
V2.1	2007-03-18	XiaoQi You	Up data Package Physical Dimension
V2.2	2007-04-23	XiaoQi You	Add Table 3-1,3-2; Up data Application Diagram, Add Pull-Up Resister R2; Add note 4;
V3.0	2007-07-16	XiaoQi You	Up data to RDA5800C; Add Application Diagram 9.4
V3.1	2007-07-21	XiaoQi You	Change some wrong in Application Diagram
V4.0	2007-10-10	XiaoQi You	Change some wrong in Notes
V4.1	2007-11-12	XiaoQi You	Change some wrong in register definition

12 Notes：

1：在使用 I^2C 模式控制芯片时，把 Pin：/SEN 直接连接到 Pin：VIO；

2：RDA5800C 支持 32.768KHz crystal oscillator 作为参考时钟输入。
（详见图 9-3,9-4）

3：可以通过硬件电路设置芯片工作在 I2C 总线控制模式。详细电路如下图：
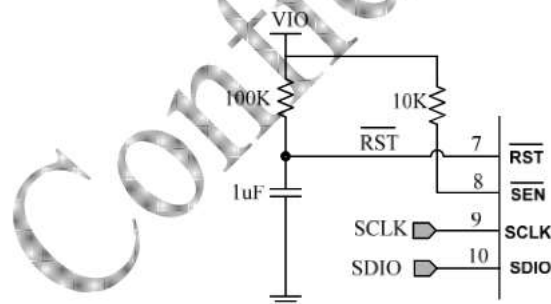
附图：I2C 总线电路接口电路

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